Amplifier instability

Erik Margan explains why an amplifier's input can be unstable – even when you follow the text-book design method.

The question of instability of an amplifier with reactive source impedance at its input that arose last year triggered memories of some 25 years ago. I remember seeing a very respectable oscilloscope burst into oscillation due to having an inductor connected to its input. I was trying to examine stray magnetic fields from a power transformer at the time.

The effect is due to the amplifier input impedance being negative over a range of frequencies. Here is an example of how even a very simple system, such as a jfet source follower, can exhibit such unexpected behaviour. **Figure1a)** shows the schematic and **1b)** the equivalent circuit. The impedance seen by the jfet source terminal is,

$$Z_S = \frac{1}{\frac{1}{R_S} + j\omega C_S} + \frac{1}{\frac{1}{R_L} + j\omega C_L} \qquad (1)$$

Summing the currents into the source node gives,

$$\frac{V_S}{Z_S} = (V_G - V_S)j\omega C_{GS} + (V_G - V_S)g_m \qquad (2)$$

From this, the small-signal transfer function at the source can be written,

$$F(\omega) = \frac{V_S}{V_G} = \frac{j\omega C_{GS} + g_m}{\frac{1}{Z_S} + j\omega C_{GS} + g_m} \qquad (3)$$

and the actual output will be scaled down by the source to load impedance ratio,

$$\frac{V_{out}}{V_G} = F(\omega)\frac{1}{Z_S\left(\frac{1}{R_L + j\omega C_L}\right)} \qquad (4)$$

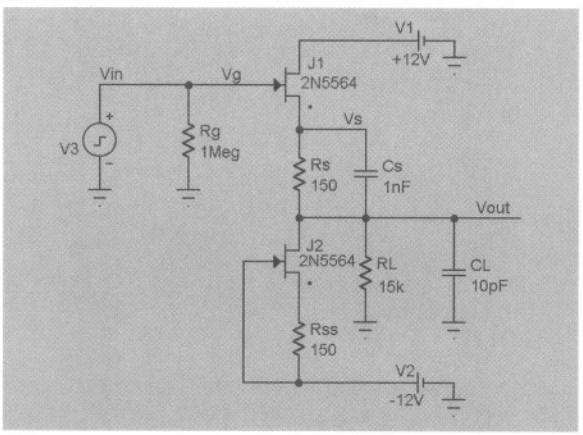
The magnitude, phase and envelope-delay of $F(\omega)$ are shown in **Fig. 2**. Note the high crosstalk in the magnitude plot at high frequencies. A cautious designer will be worried by seeing the phase plot turning upwards and the envelope-delay going positive. But there is more.

The input impedance at the jfet gate can be found by dividing the input voltage by the input current,

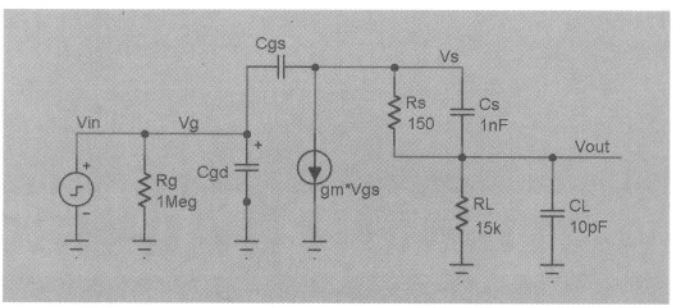
$$Z_G = \frac{V_G}{(V_G - V_S)j\omega C_{GS}} \qquad (5)$$

which results in,

$$Z_G = \frac{V_G}{(1 - F(\omega))j\omega C_{GS}} \qquad (6)$$



(a)



(b)

Fig. 1. Typical junction fet source follower, as might be used as an oscilloscope input stage.

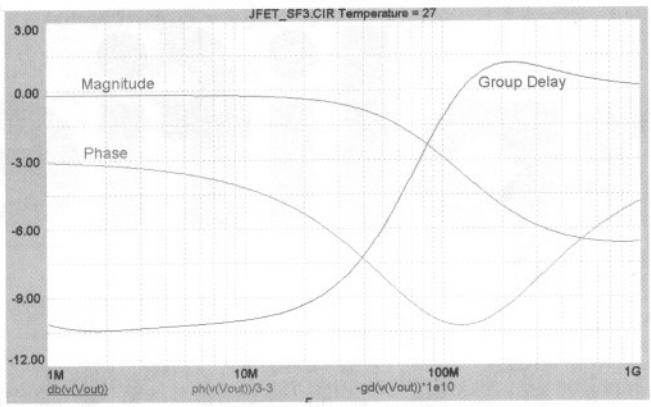


Fig. 2. Response curves of the follower in Fig. 1.

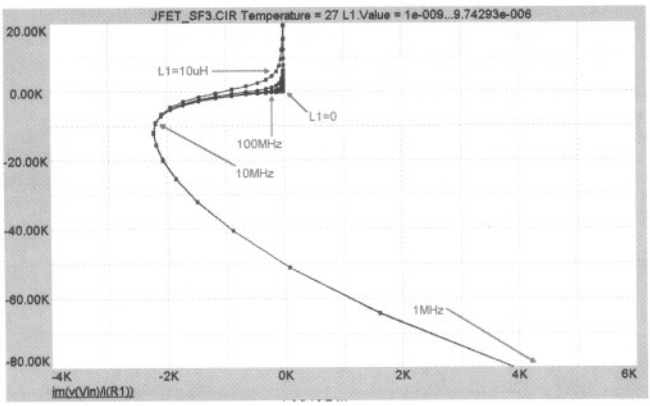


Fig. 3. Junction fet source follower input impedance for several values of input inductance.

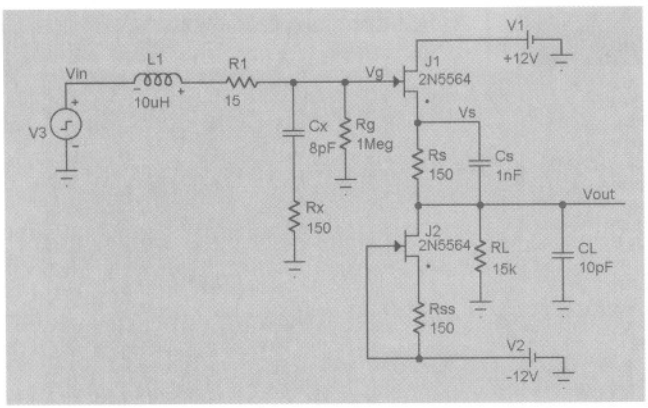


Fig. 4. Improved junction-fet source follower with negative input impedance compensation provided by R_1, R_x and C_x.

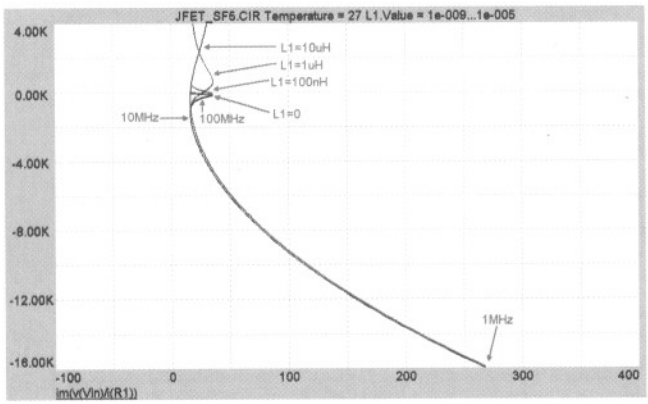


Fig. 5. Junction fet source follower input impedance for several values of L_1, compensated by R_x and C_x.

Note the negative sign, which indicates a potential source of trouble!

In parallel to Z_G there is the gate bias resistor and the gate-drain stray capacitance and any source inductance is added to the whole,

$$Z_{in} = \frac{1}{\frac{1}{Z_G} + \frac{1}{R_G} + j\omega C_{GD}} + j\omega L_1 \qquad (7)$$

The imaginary versus real part of Z_{in} is plotted in **Fig. 3**, showing that beyond 3MHz there is a negative real part, as predicted by the negative sign in the Z_G denominator. With an inductance at the input, even as low as that of a piece of wire, the circuit will oscillate at the frequency at which the Z_{in} plot crosses the negative part of the real axis.

But be warned that in too many text books Z_G is oversimplified to,

$$Z_G = Z_S + \frac{g_m Z_S + 1}{j\omega C_{GS}} \qquad (8)$$

which – since all terms are positive – shows no cause for alarm.

How to cure it

There are four solutions to this instability problem.

a) As noted in previous correspondence, the simplest method is to insert a resistor of a large-enough value – about 3kΩ – in series with the amplifier input, but this will lower the system bandwidth.

b) Choose such values of jfet source loading and transconductance, that Z_{in} remains positive, i.e. instead of using the 2N5564 one can insert the 2N5911 which has lower stray capacitances and higher source resistance, but this will also need some 300Ω in series.

c) If the input signal will come from a transducer of known inductance, it is possible to insert a small resistor in the drain of the upper jfet and thus allow some negative feedback through the gate-drain capacitance (Miller effect). This works for a limited range of inductances.

d) The best way is to add a series C_xR_x network across the input, as in **Fig. 4**, to compensate for the negative input impedance. **Fig. 5** shows the result for inductances up to 10μH. Now the series input resistance can be safely reduced to some 15Ω, without influencing the bandwidth.

With bipolar transistors, the negative input impedance is greatly reduced by the base resistance. Even so, some circuit configurations can still become unstable with input inductance. The series C_xR_x compensation can also be used here, as described for the fet. ■