3.9 JFET Source Follower

Wideband signals come usually from two source types: low impedance sources are usually those from the output of other wideband amplifiers, while medium and high impedance sources are usually those from sensors or other very low power sources.

In the first case, we employ standardized impedances, 50 Ω or 75 Ω, so that both the source and the load have the same impedance as the characteristic impedance of the cable that connects them. In this way we preserve the bandwidth and prevent reflections which would distort the signal, but we pay for this by the 50 % (−6 dB) attenuation of the signal's amplitude.

In the second case we also want a standardized value of the impedance, but this time the value is 1 MΩ, in parallel with some (inevitable) capacitance, usually 20 pF (but values from 10 to 25 pF can also be found). The standardized capacitance is helpful not only in determining the loading of the source at high frequencies, but also to allow the use of 'probes', which are actually special HF attenuators (÷10 or ÷100), so that the source can be loaded by a 10 MΩ or even a 100 MΩ resistance, while keeping the loading capacitance below some 12 pF.

With the improvement of semiconductor production processes, the so called 'active' probes have been developed, used mostly for extremely wideband signals, such as those found in modern communications and digital computers. Active probes usually have a 10 kΩ || 2 pF input impedances, with no reduction in amplitude.

The key component of both high input impedance amplifiers and active probes is the JFET (*junction field effect transistor*) source follower [Ref. 3.16].

The basic JFET source follower circuit configuration is shown in Fig. 3.9.1. In contrast to the BJT emitter follower (with an input resistance of about βR_e), the JFET source follower has a very high input resistance (between 10^9 and 10^{12} Ω), owed to the specific construction of the JFET. Its gate (a p–n junction with the drain–source channel) is reverse biased in normal operation, modulating the channel width by the electrical field only, so the input current is mainly owed to the reverse biased p–n junction leakage and the input capacitances, C_{gd} and C_{gs}.

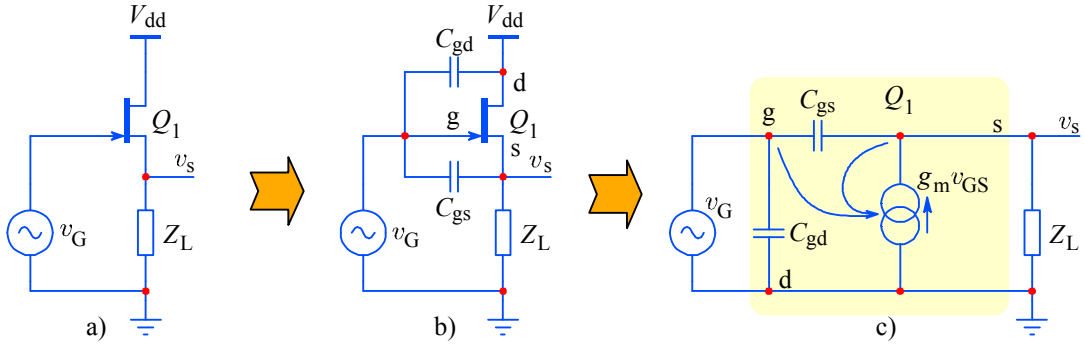

Fig. 3.9.1: The JFET source follower: a) circuit schematic; b) the same circuit, but with an ideal JFET and the inter-electrode capacitances drawn as external components; c) equivalent circuit.

A MOSFET (*metal oxide silicon field effect transistor*) has even greater input resistance (up to ~10^{15} Ω); however it also has a greater input capacitance (between 20

and 200 pF; it is also more noisy and more sensitive to damage by being overdriven), so it is not suitable for a wideband amplifier input stage.

In Fig. 3.9.1b we have drawn an ideal JFET device and its inter-electrode capacitances are modeled as external components. These capacitances determine the response at high frequencies [Ref. 3.8, 3.16, 3.20, 3.35]. Fig. 3.9.1c shows the equivalent circuit.

The source follower is actually the common drain circuit with a voltage gain of nearly unity, as the name 'follower' implies. The meaning of the circuit components is:

C_{gd} gate–drain capacitance; in most manufacturer data sheet it is labeled as C_{rss} (*common source circuit reverse capacitance*); values usually range between 1 and 5 pF;

C_{gs} gate–source capacitance; in their data sheet, manufacturers usually report the value of C_{iss}, the *common source total input capacitance*, therefore we obtain $C_{gs} \approx C_{iss} - C_{rss}$; values of C_{gs} usually range from 3 to 15 pF;

g_m JFET transconductance; usual values range between 1 000 and 15 000 µS (in some data-sheets, the symbol 'mho' is used to express that the unit *siemens* $[S] = [1/\Omega]$);

Z_L the loading impedance of the JFET source.

The JFET drain is connected to the power supply which must be a short circuit for the drain signal current, therefore we can connect C_{gd} to ground, in parallel with the signal source. We assume the signal source impedance to be zero; so we can forget about C_{gd} for a while.

From the equivalent circuit in Fig. 3.91c we find the currents for the node g:

$$i_g = v_G\, s\, C_{gd} + (v_G - v_s)\, s\, C_{gs} \tag{3.9.1}$$

and the currents for the node s:

$$(v_G - v_s)\, s\, C_{gs} + (v_G - v_s)\, g_m = \frac{v_s}{Z_L} \tag{3.9.2}$$

which can be rewritten as:

$$v_G \left(1 + \frac{g_m}{s\, C_{gs}}\right) = v_s \left(1 + \frac{g_m}{s\, C_{gs}} + \frac{1}{s\, C_{gs} Z_L}\right) \tag{3.9.3}$$

From this we obtain the system's voltage gain:

$$A_v = \frac{v_s}{v_G} = \frac{Z_L \left(1 + \dfrac{s\, C_{gs}}{g_m}\right)}{Z_L \left(1 + \dfrac{s\, C_{gs}}{g_m}\right) + \dfrac{1}{g_m}} \tag{3.9.4}$$

In practical follower circuits we want to make the output signal's dynamic range as high and the voltage gain as close to 1 as possible. The simplest way to achieve this is by replacing Z_L with a constant current generator, Fig. 3.9.2, much as we have done in

the differential amplifier. By doing this, we increase the real (resistive) part of the loading impedance, but we can do little to reduce the always present loading capacitance C_L.

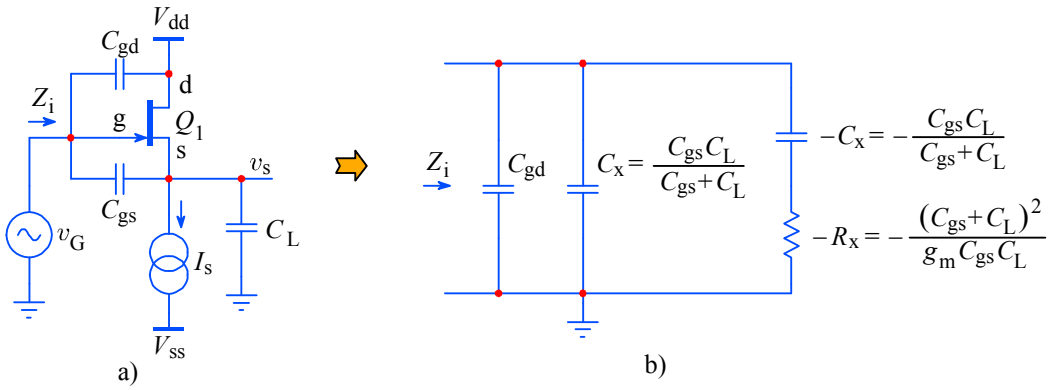

Fig. 3.9.2: The JFET source follower biased by a current generator and loaded only by the inevitable stray capacitance C_L: a) circuit schematic; b) the input impedance has two **negative** components, owed to C_{gs} and g_m (see Sec. 3.9.5).

In Eq. 3.9.4 the term C_{gs}/g_m is obviously the characteristic JFET time constant, τ_{FET}:

$$\frac{C_{gs}}{g_m} = \tau_{FET} = \frac{1}{\omega_{FET}} \tag{3.9.5}$$

Since we now have $Z_L = 1/j\omega C_L$ we can rewrite Eq. 3.9.4 as:

$$A_v = \frac{v_s}{v_G} = \frac{1 + \dfrac{j\omega}{\omega_{FET}}}{1 + j\omega\left(\dfrac{1}{\omega_{FET}} + \dfrac{C_L}{g_m}\right)} \tag{3.9.6.}$$

and by replacing g_m with $\omega_{FET}\, C_{gs}$ (Eq. 3.9.5) we obtain:

$$\frac{v_s}{v_G} = \frac{1 + \dfrac{j\omega}{\omega_{FET}}}{1 + \dfrac{j\omega}{\omega_{FET}} \cdot \dfrac{1}{D_c}} \tag{3.9.7.}$$

Here D_c is the input to output capacitive divider, which would set the output voltage if only the capacitances were in place:

$$D_c = \frac{C_{gs}}{C_{gs} + C_L} \tag{3.9.8.}$$

We would like to express Eq. 3.9.7 by its pole s_1 and zero s_2, so we need the normalized canonical form:

$$F(s) = A_0 \frac{-s_1}{s - s_1} \cdot \frac{s - s_2}{-s_2} \tag{3.9.9}$$

Therefore we replace $j\omega$ with s, multiply both the numerator and the denominator by $\omega_{\text{FET}}\, D_{\text{c}}$ and obtain:

$$F(s) = D_{\text{c}} \frac{s - (-\omega_{\text{FET}})}{s - (-\omega_{\text{FET}}\, D_{\text{c}})} \tag{3.9.10}$$

At zero frequency, the transfer function gain is:

$$A_0 = F(0) = D_{\text{c}} \frac{\omega_{\text{FET}}}{\omega_{\text{FET}}\, D_{\text{c}}} = 1 \tag{3.9.11}$$

so the zero is:

$$s_2 = -\omega_{\text{FET}} \tag{3.9.12}$$

and the pole is:

$$s_1 = -\omega_{\text{FET}}\, D_{\text{c}} \tag{3.9.13}$$

These simple relations are the basis from which we shall calculate the frequency response magnitude, the phase, the group delay and the step response of the JFET source follower (simplified at first and including the neglected components later).

3.9.1 Frequency response magnitude

The frequency response magnitude is the normalized absolute value of $F(s)$ and we want to have the normalization in both gain and frequency. Eq. 3.9.7 is already normalized in frequency (to ω_{FET}) and the gain $A_0 = 1$. To get the magnitude, we must multiply $F(j\omega)$ by its complex conjugate, $F(-j\omega)$ and take the square root:

$$|F(\omega)| = \sqrt{F(j\omega)\, F(-j\omega)} = \sqrt{\frac{1 + \dfrac{j\omega}{\omega_{\text{FET}}}}{1 + \dfrac{j\omega}{\omega_{\text{FET}}} \cdot \dfrac{1}{D_{\text{c}}}} \cdot \frac{1 - \dfrac{j\omega}{\omega_{\text{FET}}}}{1 - \dfrac{j\omega}{\omega_{\text{FET}}} \cdot \dfrac{1}{D_{\text{c}}}}}$$

$$|F(\omega)| = \sqrt{\frac{1 + \left(\dfrac{\omega}{\omega_{\text{FET}}}\right)^2}{1 + \left(\dfrac{\omega}{\omega_{\text{FET}}\, D_{\text{c}}}\right)^2}} \tag{3.9.14}$$

Since we want to examine the influence of loading we shall plot the transfer function for three different values of the ratio $C_{\text{L}}/C_{\text{gs}}$: 0.5, 1.0, and 2.0 (the corresponding values of D_{c} being 0.67, 0.5, and 0.33, respectively). The plots, shown in Fig. 3.9.3, have three distinct frequency regions: in the lower one, the circuit behaves as a voltage follower, with the JFET playing an active role, so that $v_{\text{s}} = v_{\text{G}}$, whilst in the highest frequency region, only the capacitances are important; in between we have a transition between both operating modes.

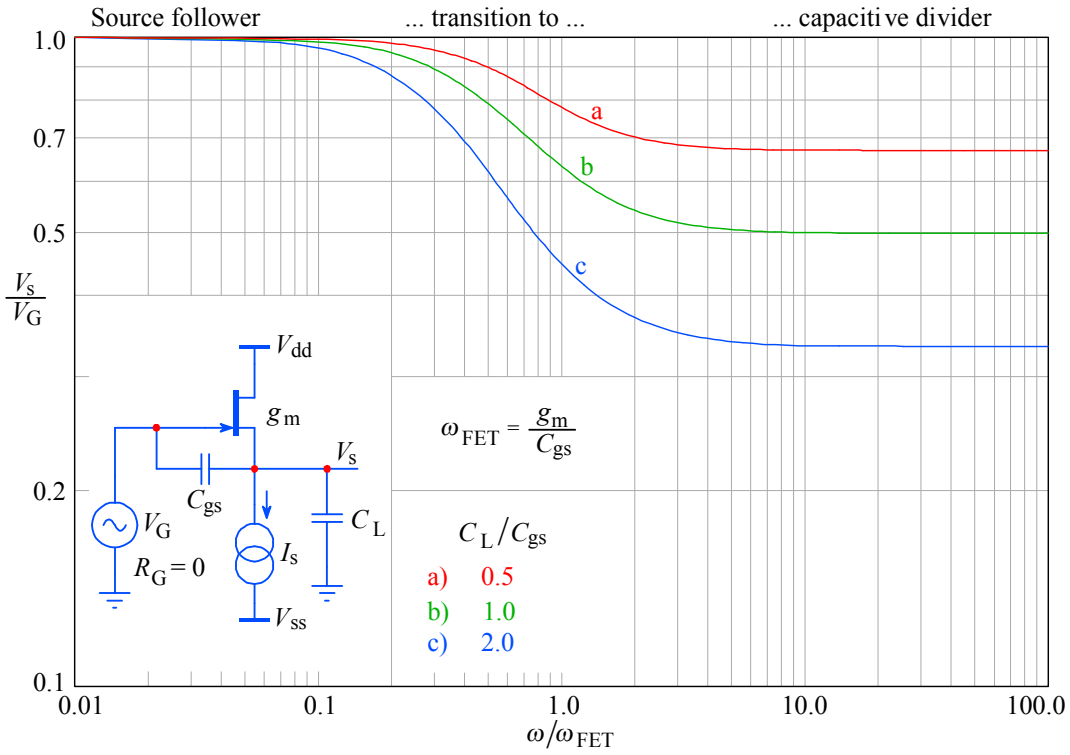

Fig. 3.9.3: Magnitude of the frequency response of the JFET source follower for three different capacitance ratios C_L/C_{gs}. The pole $s_3 = -1/R_G C_i$ has not been taken into account here (see Fig. 3.9.7 and Fig. 3.9.8).

The relation for the upper cutoff frequency is very interesting. If we set $|F(\omega)|$ to be equal to:

$$\sqrt{\frac{1+(\omega_h/\omega_{FET})^2}{1+(\omega_h/\omega_{FET}\,D_c)^2}} = \frac{1}{\sqrt{2}} \tag{3.9.15}$$

it follows that:

$$\omega_h = \omega_{FET}\,\frac{D_c}{\sqrt{1-2\,D_c^2}} \tag{3.9.16}$$

From Eq. 3.9.15 we can conclude that by putting $D_c = 1/\sqrt{2}$ the denominator is reduced to zero, thus $\omega_h = \infty$. This means that for such a capacitive ratio the magnitude never falls below $1/\sqrt{2}$. However attractive the possibility of achieving infinite bandwidth may seem, this can never be realized in practice, because any signal source will have some, although small, internal resistance R_G, resulting in an additional input pole $s_3 = -1/R_G C_i$, where C_i is the total input capacitance of the JFET. The complete transfer function will now be (see Fig. 3.9.7 and 3.9.8):

$$F(s) = \frac{s_1 s_3}{-s_2} \cdot \frac{s-s_2}{(s-s_1)(s-s_3)} \tag{3.9.17}$$

3.9.2 Phase

We obtain the phase response from Eq. 3.9.7 by taking the arctangent of the ratio of the imaginary to the real part of $F(j\omega)$:

$$\varphi(\omega) = \arctan \frac{\Im\{F(j\omega)\}}{\Re\{F(j\omega)\}} \tag{3.9.18}$$

Since in Eq. 3.9.7 we have a single real pole an a single real zero, the resulting phase angle is calculated as:

$$\varphi(\omega) = \arctan \frac{\omega}{\omega_{\mathrm{FET}}} - \arctan \frac{\omega}{\omega_{\mathrm{FET}}\, \mathrm{D_c}} \tag{3.9.19}$$

In Fig. 3.9.4 the three phase plots with same C_L/C_{gs} ratios are shown. Because of the zero, the phase returns to the initial value at high frequencies.

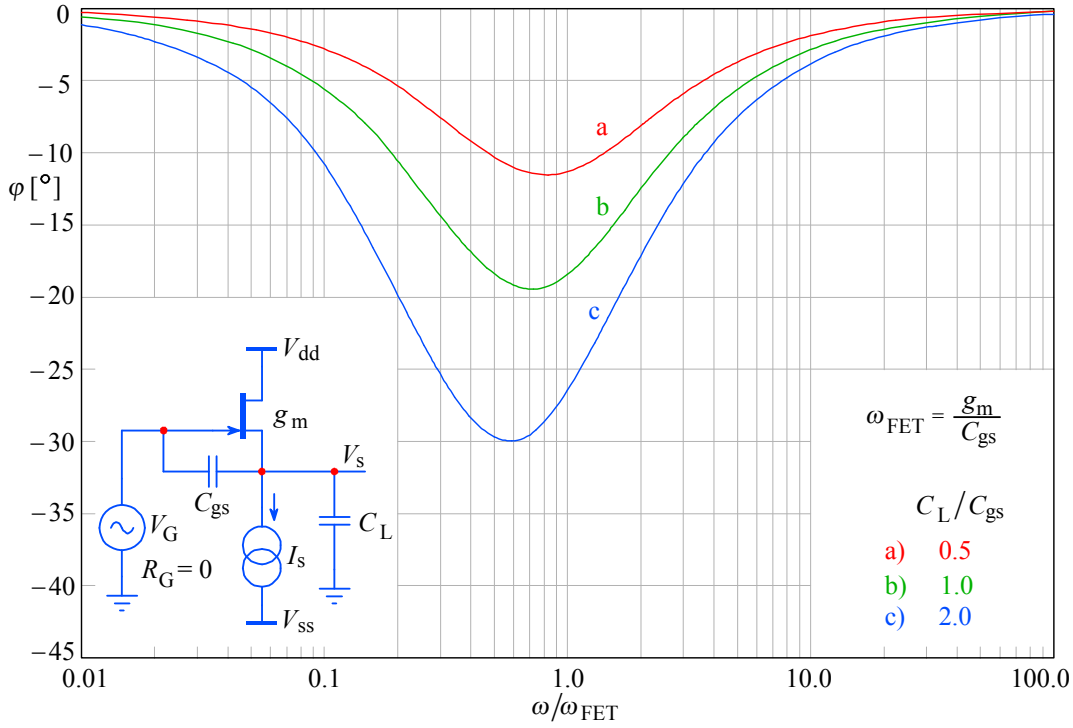

Fig. 3.9.4: Phase plots of the JFET source follower for the same three capacitance ratios.

3.9.3 Envelope delay

We obtain the envelope delay by taking the ω derivative of the phase:

$$\tau_e = \frac{d\varphi}{d\omega} \tag{3.9.20}$$

but we usually prefer the normalized expression $\tau_e\, \omega_h$. In our case, however, the upper cut off frequency, ω_h, is changing with the capacitance divider D_c. So instead of ω_h we

shall, rather, normalize the envelope delay to the characteristic frequency of the JFET itself, ω_{FET}:

$$\tau_e\,\omega_{FET} = \frac{1}{1+(\omega/\omega_{FET})^2} - \frac{D_c}{D_c^2+(\omega/\omega_{FET})^2} \tag{3.5.21}$$

The envelope delay plots for the three capacitance ratios are shown in Fig. 3.9.5. Note that for all three ratios there is a frequency region in which the envelope delay becomes **positive**, implying that the output signal advance, in correlation with the phase plots, goes up with frequency. We have explained the physical background of this behavior in Part 2, Fig. 2.2.5, 2.2.6. The positive envelope delay influences the input impedance in a very unfavorable way, as we shall soon see.

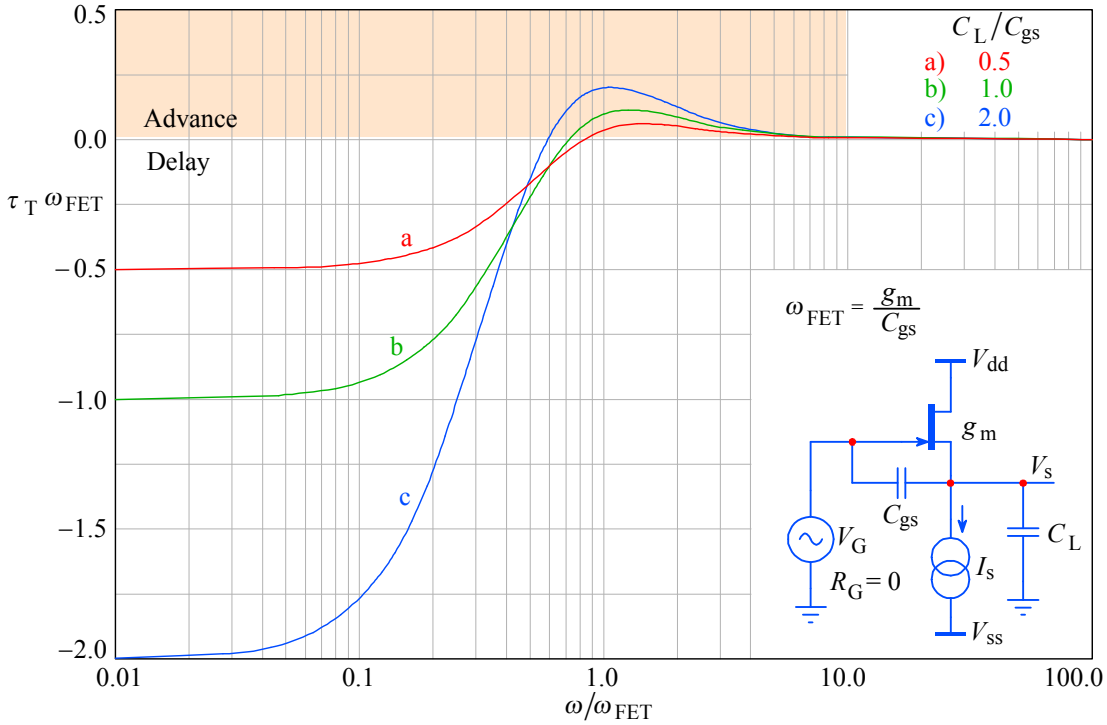

Fig. 3.9.5: The JFET envelope delay for the three capacitance ratios. Note the positive peak (phase advance region): trouble in sight!

3.9.4 Step response

We are going to use Eq. 3.9.9, which we multiply by the unit step operator $1/s$ to obtain the step response in the complex frequency domain; we then obtain the time domain response by applying the inverse Laplace transform:

$$G(s) = \frac{1}{s}\,F(s) = \frac{1}{s}\,D_c\,\frac{s-s_2}{s-s_1} \tag{3.9.22}$$

$$g(t) = \mathcal{L}^{-1}\{G(s)\} = D_c \sum_{s=0}^{s_1} \operatorname{res} \frac{(s-s_2)\,e^{st}}{s\,(s-s_1)} \tag{3.9.23}$$

The residue at $s \to 0$ is:

$$\text{res}_0 = \lim_{s \to 0} s \frac{(s - s_2)\, e^{st}}{s\,(s - s_1)} = \frac{s_2}{s_1} \tag{3.9.24}$$

and the residue at $s \to s_1$ is:

$$\text{res}_1 = \lim_{s \to s_1} (s - s_1) \frac{(s - s_2)\, e^{st}}{s\,(s - s_1)} = \frac{s_1 - s_2}{s_1}\, e^{s_1 t} \tag{3.9.25}$$

By entering both residues back into Eq. 3.9.23 we get:

$$g(t) = D_c \left(\frac{s_2}{s_1} + \frac{s_1 - s_2}{s_1}\, e^{s_1 t} \right) \tag{3.9.26}$$

and, by considering Eq. 3.9.12 and 3.9.13, as well as that $\omega_{FET} = 1/\tau_{FET}$ and using the normalized time t/τ_{FET}, we end up with:

$$g(t) = 1 - (1 - D_c)\, e^{-D_c t/\tau_{FET}} \tag{3.9.27}$$

The plot of this relation is shown in Fig. 3.9.6, again for the same three capacitance ratios. The initial output signal jump at $t = 0$ is the input signal cross-talk (through C_{gs}) multiplied by the D_c factor:

$$g(0) = D_c \tag{3.9.28}$$

Following the jump is the exponential relaxation towards the normal follower action at lower frequencies. If the input pole $s_3 = -1/R_G C_i$ is taken into account, the jump would be slowed down to an exponential rise with a time constant of $R_G C_i$.

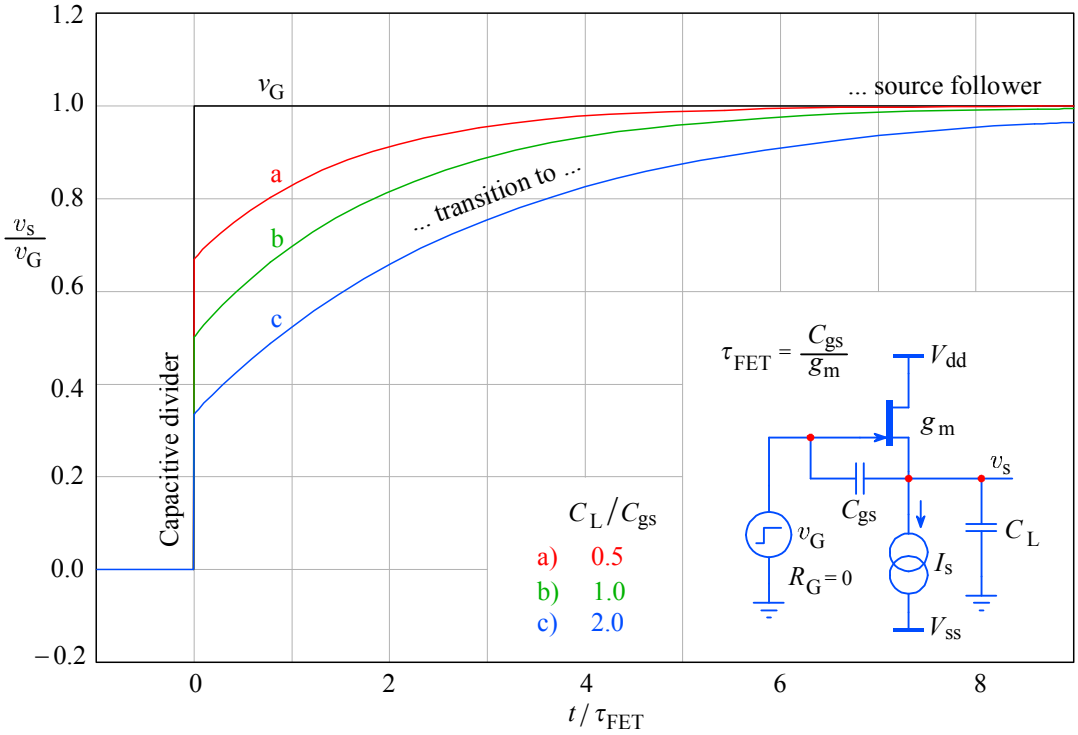

Fig. 3.9.6: The JFET source follower step response for the three capacitance ratios.

As mentioned earlier in connection with Eq. 3.9.17, when the value of R_G is comparable to $1/g_m$, an additional pole has to be to considered. We must derive the system transfer function again, from the following two equations:

For the currents into the node g:

$$\frac{v_G - v_g}{R_G} = \frac{v_g}{\frac{1}{s\,C_{gd}}} + \frac{v_g - v_s}{\frac{1}{s\,C_{gs}}} \tag{3.9.29}$$

and for the currents into the node s:

$$\frac{v_g - v_s}{\frac{1}{s\,C_{gs}}} + (v_g - v_s)\,g_m = \frac{v_s}{\frac{1}{s\,C_L}} \tag{3.9.30}$$

We first express v_g as a function of v_s from Eq. 3.9.30:

$$v_g = v_s\left(1 + \frac{s\,C_L}{s\,C_{gs} + g_m}\right) \tag{3.9.31}$$

Then we replace v_g in Eq. 3.9.29 by 3.9.31:

$$v_G = v_s\left(1 + \frac{s\,C_L}{s\,C_{gs} + g_m}\right)(1 + R_G\,s\,C_{gd} + R_G\,s\,C_{gs}) - v_s R_G\,s\,C_{gs} \tag{3.9.32}$$

After some further manipulation we arrive at:

$$\frac{v_s}{v_G} = \frac{1}{1 + R_G\,s\,C_{gd} + \frac{s\,C_L}{s\,C_{gs} + g_m}(1 + R_G\,s\,(C_{gd} + C_{gs}))} \tag{3.9.33}$$

Now we put this into the normalized canonical form and use Eq. 3.9.5 again to replace the term g_m/C_{gs} with ω_{FET}. Also, we express all the time constants as functions of ω_{FET} and the appropriate capacitance ratios. Finally, we want to see how the response depends on the product $g_m R_G$, so we multiply all the terms containing R_G with g_m and compensate each of them accordingly. The final expression is:

$$\frac{v_s}{v_G} = \frac{(s + \omega_{FET})\frac{1}{g_m R_G} \cdot \frac{\omega_{FET}\,\frac{C_{gs}}{C_{gd}}}{\left(1 + \frac{C_L}{C_{gs}} + \frac{C_L}{C_{gd}}\right)}}{s^2 + s\,\frac{\omega_{FET}\left[1 + \frac{1}{g_m R_G}\left(\frac{C_{gs}}{C_{gd}} + \frac{C_L}{C_{gd}}\right)\right]}{\left(1 + \frac{C_L}{C_{gs}} + \frac{C_L}{C_{gd}}\right)} + \frac{1}{g_m R_G} \cdot \frac{\omega_{FET}^2\,\frac{C_{gs}}{C_{gd}}}{\left(1 + \frac{C_L}{C_{gs}} + \frac{C_L}{C_{gd}}\right)}} \tag{3.9.34}$$

To plot the responses we shall set:

$$\frac{C_L}{C_{gs}} = 1, \qquad \frac{C_{gs}}{C_{gd}} = 5, \qquad \omega_{FET} = 1, \qquad s = j\omega, \qquad \text{and} \qquad g_m R_G = [0.3,\ 1,\ 3]$$

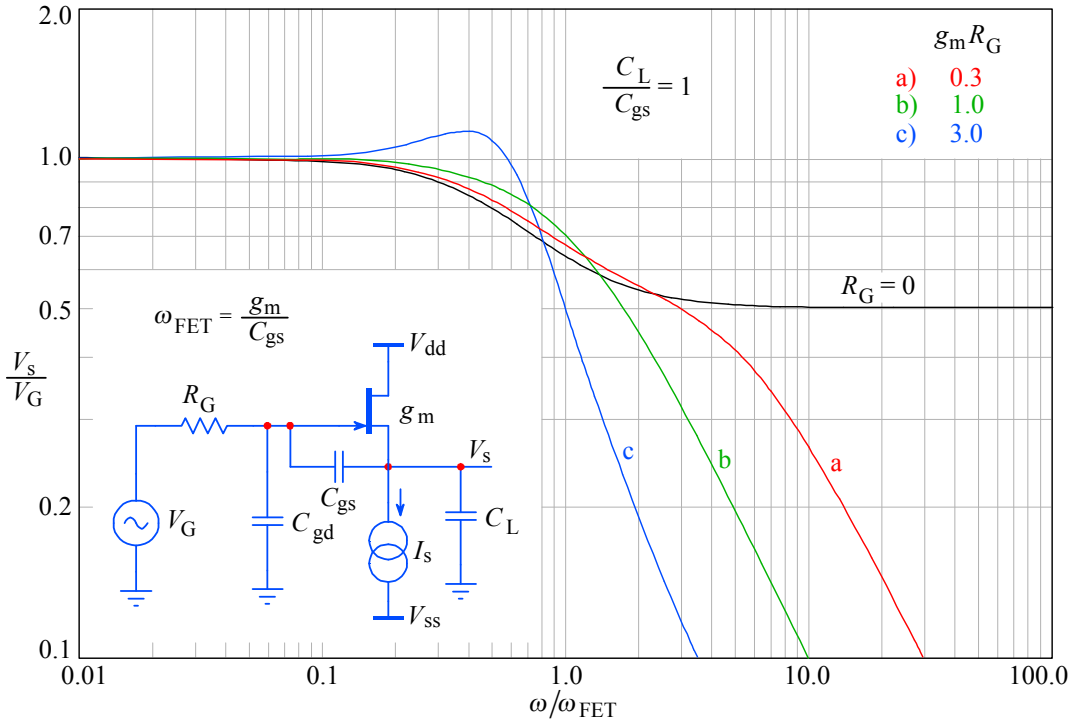

Fig. 3.9.7: The JFET source follower frequency response for a ratio $C_L/C_{gs} = 1$ and a variable signal source impedance, so that $R_G g_m$ is 0.3, 1, and 3, respectively. Note the response peaking for $g_m R_G = 3$.

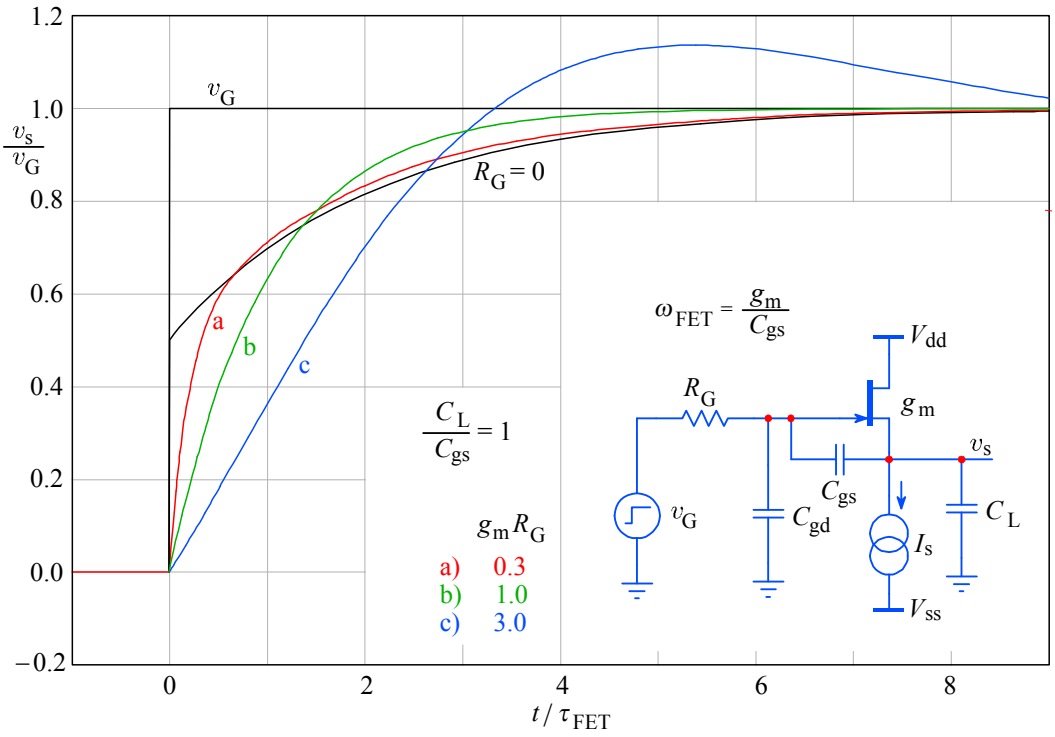

Fig. 3.9.8: The JFET source follower step response for the same conditions as in Fig. 3.9.7.

3.9.5 Input impedance

In Fig. 3.9.7 and 3.9.8 we have seen how the JFET source follower response is affected by its input impedance; this behavior becomes evident when the signal source has a non-zero resistance. Here, we are going to explore the circuit in more depth to examine the influence of a complex and, in particular, inductive signal source.

As we have done in the previous analysis, the gate–drain capacitance C_{gd} will appear in parallel with the input, so we can treat its admittance separately and concentrate on the remaining input components.

We start from Eq. 3.9.1 by solving it for v_s:

$$v_s = v_G - \frac{i_i}{s\,C_{gs}} \tag{3.9.35}$$

This we insert into Eq. 3.9.2:

$$-v_G\,(s\,C_{gs} + g_m) + \left(v_g - \frac{i_i}{s\,C_{gs}}\right)\left(s\,C_{gs} + g_m + \frac{1}{Z_L}\right) = 0 \tag{3.9.36}$$

Because the JFET source is biased from a constant current generator (whose impedance we assume to be infinite) the loading admittance is $1/Z_L = s\,C_L$. Let us put this back into Eq. 3.3.36 and rearrange it a little:

$$v_G\,s\,C_L = i_i\left(1 + \frac{g_m}{s\,C_{gs}} + \frac{C_L}{C_{gs}}\right) \tag{3.9.37}$$

Furthermore:

$$v_G = i_i\left(\frac{1}{s\,C_L} + \frac{g_m}{s^2\,C_{gs}\,C_L} + \frac{1}{s\,C_{gs}}\right)$$

$$= i_i\,\frac{s\,(C_{gs} + C_L) + g_m}{s^2\,C_{gs}\,C_L} \tag{3.9.38}$$

The input impedance (without C_{gd}, hence the prime [$'$]) is then:

$$Z_i' = \frac{v_g}{i_i} = \frac{s\,(C_{gs} + C_L) + g_m}{s^2\,C_{gs}\,C_L} \tag{3.9.39}$$

To see more clearly how this impedance is comprised, we invert it to find the admittance and apply the continuous fraction synthesis in order to identify the individual components.

$$Y_i' = \frac{s^2\,C_{gs}\,C_L}{s\,(C_{gs} + C_L) + g_m} = s\,\frac{C_{gs}\,C_L}{C_{gs} + C_L} - \frac{g_m\,s\,\dfrac{C_{gs}\,C_L}{C_{gs} + C_L}}{s\,(C_{gs} + C_L) + g_m} \tag{3.9.40}$$

The first fraction is the admittance of the capacitances C_{gs} and C_L connected in series. Let us name this combination C_x:

$$C_x = \frac{C_{gs}\,C_L}{C_{gs} + C_L} \tag{3.9.41}$$

The second fraction, which has a negative sign, must be further simplified. We invert it again, and after some simple rearrangement we obtain the impedance:

$$Z_x = -\frac{(C_{gs}+C_L)^2}{g_m C_{gs} C_L} - \frac{C_{gs}+C_L}{s C_{gs} C_L} \tag{3.9.42}$$

The first part is interpreted as a negative resistance, which we shall label $-R_x$ in order to follow the negative sign in the following analysis more clearly:

$$-R_x = -\frac{(C_{gs}+C_L)^2}{g_m C_{gs} C_L} \tag{3.9.43}$$

The second part as a negative capacitance, which we label $-C_x$ because it has the same absolute value as C_x from the Eq. 3.9.41:

$$-C_x = -\frac{C_{gs} C_L}{C_{gs}+C_L} \tag{3.9.44}$$

Now that we have all the components we can reintroduce the gate–drain capacitance C_{gd}, so that the final equivalent input impedance looks like Fig. 3.9.9. We can write the complete input admittance:

$$Y_i = j\omega (C_{gd}+C_x) - \frac{1}{R_x + \dfrac{1}{j\omega C_x}} \tag{3.9.45}$$

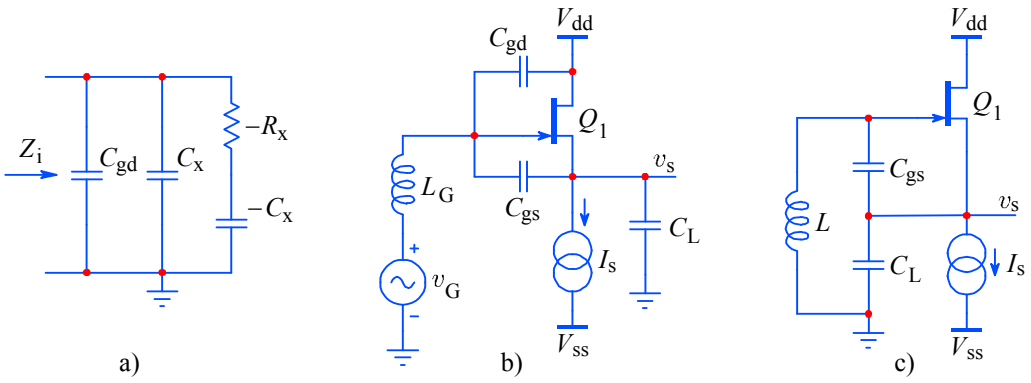

Fig. 3.9.9: a) The equivalent input impedance of the capacitively loaded JFET source follower has negative components which can be a nuisance if, as in b), the signal source has an inductive impedance, forming c) a familiar Colpitts oscillator. If C_{gd} is small, the circuit will oscillate for a broad range of inductance values.

We can separate the real and imaginary part of Y_i by putting Eq. 3.9.45 on a common denominator:

$$Y_i = \Re\{Y_i\} + \Im\{Y_i\}$$

$$= -\frac{\omega^2 C_x^2 R_x}{1+\omega^2 C_x^2 R_x^2} + j\omega \frac{C_{gd}+\omega^2 C_x^2 R_x^2 (C_{gd}+C_x)}{1+\omega^2 C_x^2 R_x^2} \tag{3.9.46}$$

The negative real part can cause some serious trouble [Ref. 3.24]. Suppose we are troubleshooting a circuit with a switching power supply and we suspect it to be a cause of a strong electromagnetic interference (EMI); we want to use a coil with an appropriate inductance L (which, of course, has its own real and imaginary admittance) to inspect the various parts of the circuit for EMI intensity and field direction. If we connect this coil to the source follower and if the coil resistance is low, we would have:

$$\Re\{Y_L\} + \Re\{Y_\mathrm{i}\} \leq 0 \tag{3.9.47}$$

and the source follower becomes a familiar Colpitts oscillator, Fig. 3.9.9c [Ref. 3.25]. Indeed, some older oscilloscopes would burst into oscillation if connected to such a coil and with its input attenuator switched to maximum sensitivity (a few highly priced instruments built by respectable firms, back in early 1970's, were no exception).

By taking into account Eq. 3.9.42, 3.9.43 and 3.9.9 and substituting $\omega_\mathrm{FET} = g_\mathrm{m}/C_\mathrm{gs}$, the real part of the input impedance can be rewritten as:

$$\Re(Y_\mathrm{i}) = G_\mathrm{i} = -g_\mathrm{m}\,\frac{C_\mathrm{L}}{C_\mathrm{gs}} \cdot \frac{(\omega/\omega_\mathrm{FET})^2}{1 + (\omega/\omega_\mathrm{FET}\,D_\mathrm{c})^2} \tag{3.9.48}$$

The last fraction represents the normalized frequency dependence of this admittance:

$$G_\mathrm{iN} = \frac{(\omega/\omega_\mathrm{FET})^2}{1 + (\omega/\omega_\mathrm{FET}\,D_\mathrm{c})^2} \tag{3.9.49}$$

Fig. 3.9.10 shows the plots of G_iN for the same ratios of $C_\mathrm{L}/C_\mathrm{gs}$ as before. Note the quadratic dependence (of D_c) at high frequencies.

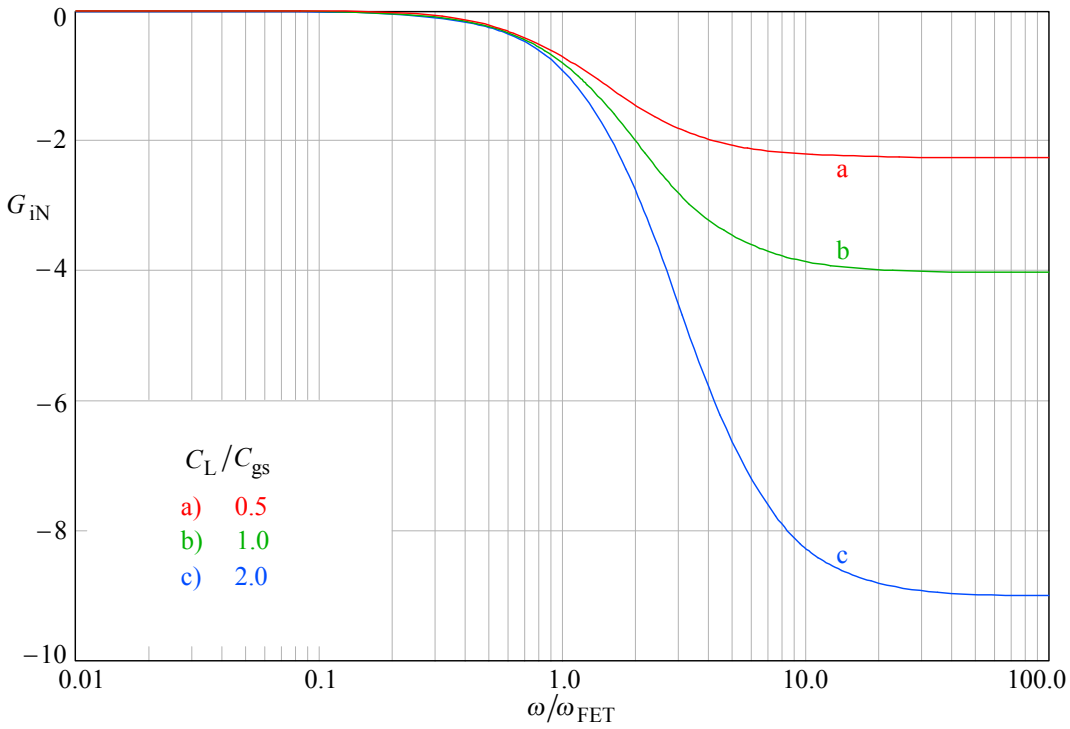

Fig. 3.9.10: Normalized negative input conductance G_iN vs. frequency.

A negative input impedance is always highly undesirable and we shall show a few possible solutions. The obvious way would be to introduce a resistor in series with

the JFET gate; since we should have some series resistance anyway in order to protect the sensitive input from static discharge or accidental overdrive, this will seem to be the preferred choice. However, after a closer look, this protection resistance is too small to prevent oscillations in case of an inductive signal source impedance. The required resistance value which will guarantee stability in all conditions will be so high that the bandwidth will be reduced by nearly an order of magnitude. Thus this method of compensation is used only if we do not care how much bandwidth we obtain.

A more elegant method of compensation is the one which we have used already in Fig. 3.5.3. If we introduce a serially connected $R_x C_x$ network in parallel with the JFET input, as shown in Fig. 3.9.11, we obtain $Y_x = 0$ and $Z_x = \infty$. Note the corresponding phasor diagram: we first draw the negative components, $-R_x$ and $-C_x$, find the impedance vector $-Z_x$ and invert it to find the negative admittance, $-Y_x$. We then compensate it by a positive admittance Y_x such that their sum $Y_{ic} = 0$. We finally invert Y_x to find Z_x and decompose it into its real and imaginary part, R_x and C_x:

$$Y_{ic} = \frac{1}{-R_x - \dfrac{1}{j\omega C_x}} + \frac{1}{R_x + \dfrac{1}{j\omega C_x}} = 0 \qquad (3.9.50)$$

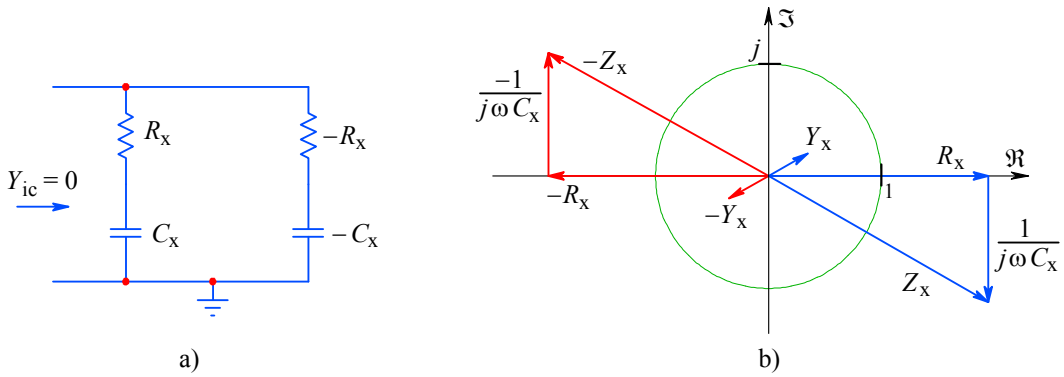

Fig. 3.9.11: a) The negative components of the input impedance can be compensated by an equal but positive network, connected in parallel, so that their admittances sum to zero (infinite impedance). In b) we see the corresponding phasor diagram.

With this compensation, the total input impedance is the one belonging to the parallel connection of C_{gd} with C_x and assuming a 1 MΩ gate bias resistor R_{in}:

$$Z_i = \frac{1}{\dfrac{1}{R_{in}} + j\omega(C_{gd} + C_x)} = \frac{R_{in}}{1 + j\omega\left(C_{gd} + \dfrac{C_{gs}\,C_L}{C_{gs} + C_L}\right)R_{in}} \qquad (3.9.51)$$

The analysis of the input impedance would be incomplete without Fig. 3.9.12, where the Nyquist diagrams of the impedance are shown revealing its frequency dependence, as well as the influence of different signal source impedances.

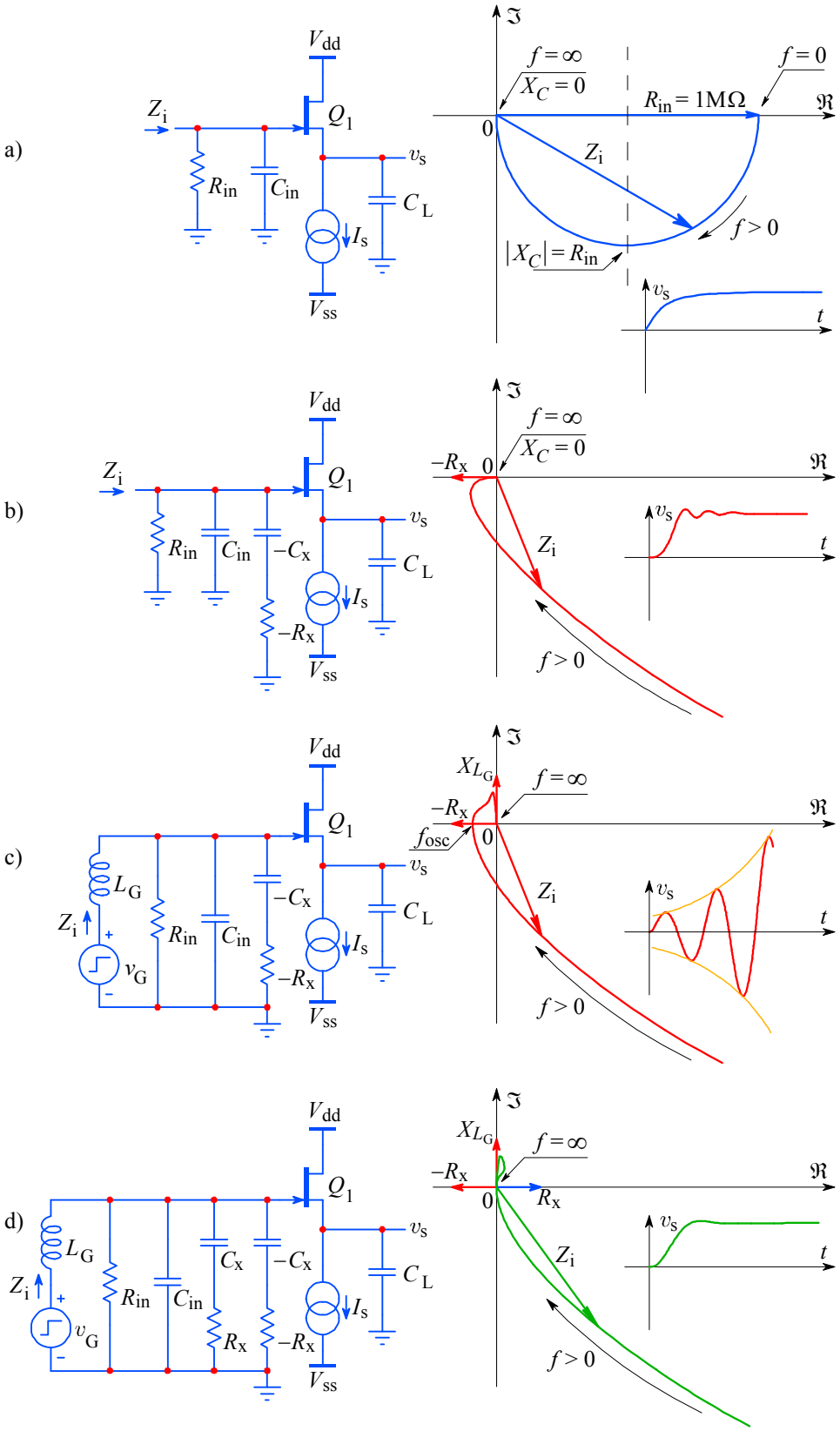

Fig. 3.9.12: **a)** The input impedance of the JFET source follower, assumed to be purely capacitive and in parallel with a 1 MΩ gate biasing resistor; thus at $f = 0$ we see only the resistor and at $f = \infty$ the reactance of the input capacitance is zero; **b)** the negative input impedance components affect the input impedance near the origin; **c)** with an inductive signal source, the point in which the impedance crosses the negative real axis corresponds to the system resonant frequency, provoking oscillations. **d)** The compensation removes the negative components.

In Fig. 3.9.12a the JFET gate is tied to ground by a 1 MΩ resistor, which, with a purely capacitive input impedance, would give a phasor diagram in the form of a half circle with frequency varying from DC to infinity.

In Fig. 3.9.12b we concentrate on the small area near the complex plane origin (high frequencies, close to f_{FET}), where we draw the influence of the negative input impedance components, assuming a resistive signal source.

In Fig. 3.9.12c an inductive signal source (with a small resistive component) will cause the impedance crossing the real axis in the negative region, therefore the circuit would oscillate at the frequency at which this crossing occurs.

Finally, in Fig. 3.9.12d we see the same situation but with the negative components compensated as in Fig. 3.9.11. Note the small loop in the first quadrant of the impedance plot — it is caused by the small resistance R_G of the coil L_G, the coil inductance, and the total input capacitance C_{in}.

In Fig. 3.9.13 we see yet another way of compensating the negative input impedance. Here the compensation is achieved by inserting a small resistance R_d in the drain, thus allowing the anti-phase signal at the drain to influence the gate via C_{gd} and cancel the in-phase signal from the JFET source via C_{gs}. This method is sometimes preferred over the former method, because the PCB pads, which are needed to accommodate the additional compensation components, also create some additional parasitic capacitance from the gate to ground.

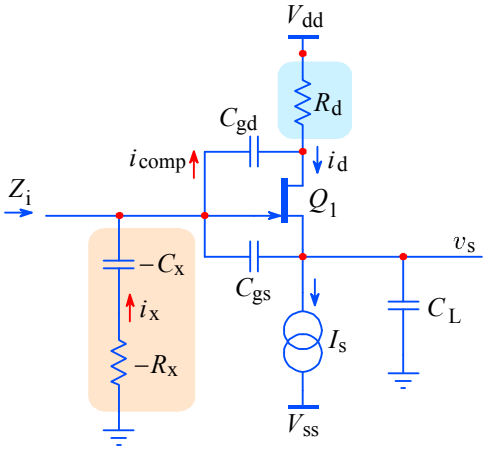

Fig. 3.9.13: Alternative compensation of the input impedance negative components, using negative feedback from the JFET drain.

It should be noted, however, that the negative input impedance compensation can be achieved for small signals only. Large signals vary the JFET gate's reverse bias voltage and the drain–source voltage considerably, therefore both C_{gs} and C_{gd}, as well as g_m, change with voltage. We therefore expect some nonlinear effects to appear with a large signal drive. We shall examine this and some other aspects of the source follower's performance in Part 5.